



LC6527N/F/L, 6528N/F/L

Single Chip 4-Bit Microcontroller for Small-Scale Control-Oriented Applications

The LC6527N / F / L, LC6528N / F / L belong to our single-chip 4-bit microcontroller LC6500 series fabricated using CMOS process technology and are suited for use in small-scale control-oriented applications. Their basic architecture and instruction set are the same. Application areas include the standard logic circuits and applications where the number of controls is small. The LC6527N / F / L, LC6528N / F / L have relation to the LC6527C / H, LC6528C / H. The C version can be replaced by N version, and the H version (a part of the function is different). The L version is added as a low voltage version. The following show the careful difference of C and N version when you replace C version with N version.

		C version	N version
Operating Temperature		-30°C to +70°C	-40°C to +85°C
1-pin C oscillation		exist	not exist
CF Oscillation Constant	400kHz MURATA	C1=C2=330pF R=0Ω	C1=C2=220pF R=2.2kΩ
	800kHz MURATA	C1=C2=220pF R=0Ω	C1=C2=100pF R=2.2kΩ
		KYOCERA	C1=C2=220pF R=0Ω
	1MHz MURATA	C1=C2=220pF R=0Ω	C1=C2=100pF R=2.2kΩ

(Note) The suffix of recommend oscillation is changed C version and N version, but the characteristic is no change.

Features

- 1) CMOS technology for a low-power operation (with instruction-controlled standby function)
- 2) ROM / RAM
LC6527N / F / L ROM : 1K × 8bits, RAM : 64 × 4bits
LC6528N / F / L ROM : 0.5K × 8bits, RAM : 32 × 4bits
- 3) Instruction set : 51 kinds selectable from 80 instructions common to the LC6500 series
- 4) Wide operating voltage range from 2.2V to 6.0V (L version)
- 5) Instruction cycle time of 0.92μs (F version)

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LC6527N/F/L, 6528N/F/L

6) Flexible I / O port

- Number of ports : 4 ports / 13 pins max.
- All ports : Input / output common
Input / output voltage 15V max. (open drain type)
Output current 20mA max. (sink current) (LED direct drivable)
- Option selectable for your intended system
 - A. Open drain output, pull-up resistor : Single-bit select for all ports
 - B. Output level at the reset mode : 4-bit select of H / L level for port C / D

7) Stack level : 4 levels

8) Timer : 4-bit prescaler+8-bit programmable timer

9) Clock oscillation option selectable for your intended system

- Oscillator option : 2-pin RC oscillation (N, L version)
2-pin ceramic resonator oscillation, 1-pin external clock input (N, F, L version)
- Predivider option : No predivider, 1 / 3 predivider, 1 / 4 predivider (N, L version)

Function Table

Item		LC6527N / 28N	LC6527F / 28F	LC6527L / 28L
Memory	ROM	1024 × 8 bits (27N) 512 × 8 bits (28N)	1024 × 8 bits (27F) 512 × 8 bits (28F)	1024 × 8 bits (27L) 512 × 8 bits (28L)
	RAM	64 × 4 bits (27N) 32 × 4 bits (28N)	64 × 4 bits (27F) 32 × 4 bits (28F)	64 × 4 bits (27L) 32 × 4 bits (28L)
Instruction	Instruction set	51	51	51
On-chip function	Timer	4-bit prescaler+8-bit timer	4-bit prescaler+8-bit timer	4-bit prescaler+8-bit timer
	Stack level	4	4	4
	Standby function	Standby available by HALT instruction	Standby available by HALT instruction	Standby available by HALT instruction
Input / output port	Number of ports	I / O 13 max.	I / O 13 max.	I / O 13 max.
	I / O voltage	15V max.	15V max.	15V max.
	Output current	10mA typ. 20mA max.	10mA typ. 20mA max.	10mA typ. 20mA max.
	I / O circuit configuration	Open drain (N-channel) or pull-up resistor-provided output selectable bit by bit.		
	Output level at reset mode	“H” or “L” level selectable port by port (port C, D only)		
Characteristic	Minimum cycle time	2.77μs (VDD≥4V) 6.0μs (VDD≥3V)	0.92μs (VDD≥4.5V)	3.84μs (VDD≥2.2V)
	Supply voltage	3 to 6V	4.5 to 6V	2.2 to 6V
	Current dissipation	2.5mA typ.	4mA typ.	2.5mA typ.
Oscillation	Resonator	RC (850kHz, 400kHz typ.) ceramic (400k, 800k, 1MHz, 4MHz)	ceramic 4MHz	RC (400kHz typ.) ceramic (400k, 800k, 1MHz, 4MHz)
	predivider option	1 / 1, 1 / 3, 1 / 4	1 / 1	1 / 1, 1 / 3, 1 / 4
Other	Package	DIP18, MFP18*	DIP18, MFP18*	DIP18, MFP18*

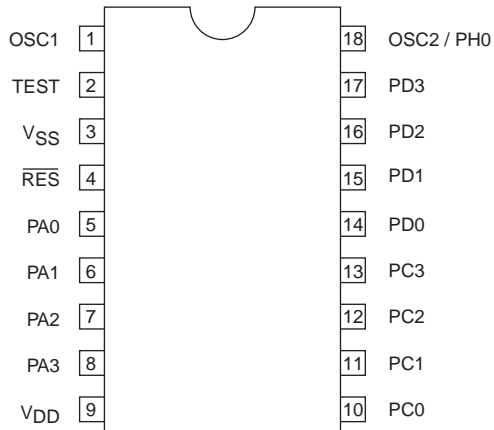
(Note) Information on the resonator and oscillation circuit constants will be presented as soon as the recommended circuit is determined.

*MFP18 : under development

LC6527N/F/L, 6528N/F/L

Pin Assignment

LC6527N / F / L
LC6528N / F / L

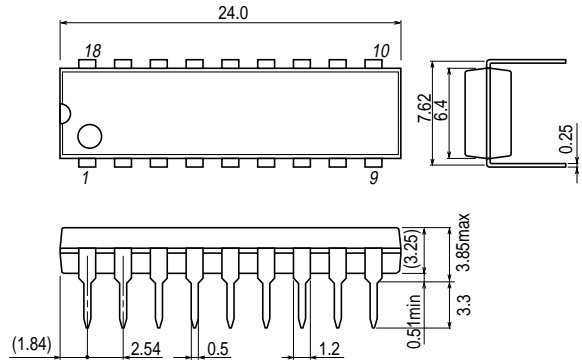


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Common to DIP • MFP

Package Dimentions

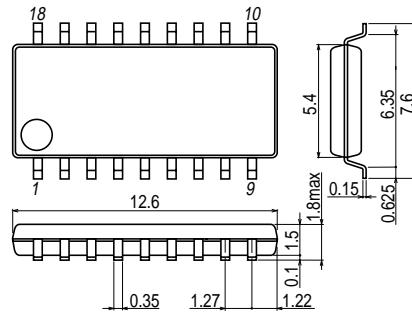
unit : mm
3007B



SANYO : DIP18(300mil)

unit : mm
3095

- Do not immerse the package in the solder dip tank when mounting the MFP on the substrate.



SANYO : MFP-18(300mil)

(Note) The package is the reference figure without the description of the rank. Please inquire us for the formal package.

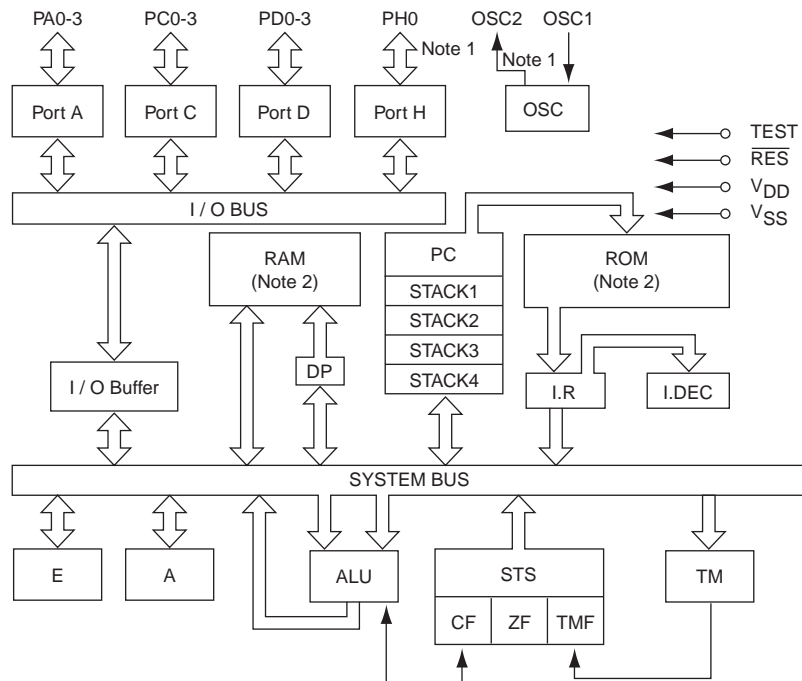
LC6527N/F/L, 6528N/F/L

Pin Name

OSC1, OSC2 : R, C or ceramic resonator for OSC	PH0 : Input / output common port H 0
$\overline{\text{RES}}$: Reset	TEST : Test
PA 0-3 : Input / output common port A 0-3	
PC 0-3 : Input / output common port C 0-3	
PD 0-3 : Input / output common port D 0-3	

System Block Diagram

LC6527N / F / L, LC6528N / F / L



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Note1. The PH0 pin or OSC2 pin is selected by the mask option.

Note2. LC6527N / F / N	ROM : 1024 bytes	RAM : 64 words
LC6528N / F / N	ROM : 512 bytes	RAM : 32 words

Development Support Tools

The following are available to support the program development for the LC6527, LC6528.

(1) User's Manual

“LC6527, LC6528 User's Manual” No. 24-6016 ('86.10.1.)

Note : Do not use “LC6523 Series User's Manual” No.16A-7015 and No.16-9064.

(2) Development Tool Manual

For the EVA-800 or the EVA-850 system, refer to “EVA-800. LC6527, LC6528 Development Tool Manual”.

(3) Development Tools

A. For program evaluation

1. Piggy back (LC65PG23 / 26)

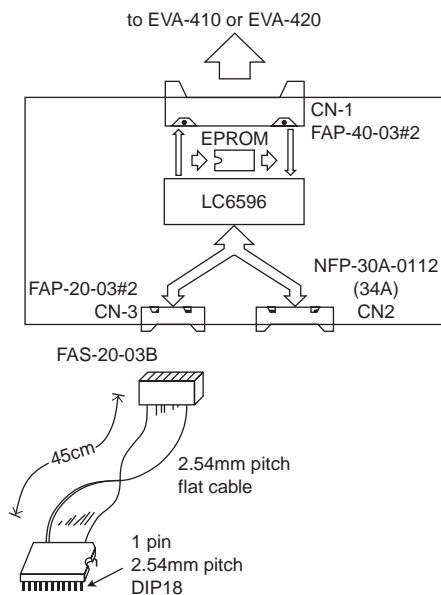
2. 23T27 ; The pin-to-pin conversion socket for the piggy back LC65PG23 / 26.

B. EVA-86000 system for program development is on development.

C. For program evaluation

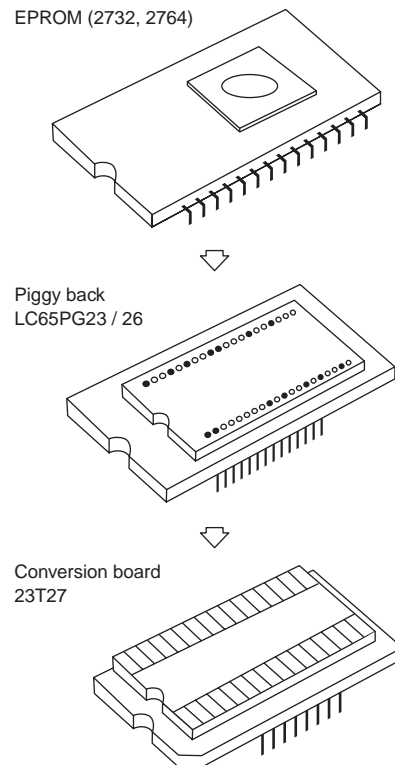
microcontroller built-in EPROM (LC65E29)+conversion substrate (29T027)

Note. For notes for program evaluation, do not fail to refer to '4-3. Notes when evaluating programs' in “LC6527, LC6528 User's Manual”.



FGP-20-01#2 removed the 10 pin and 11 pin can be used for the DIP18.

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ILC00142

Fig.1 Evaluation kit target board
(EVA-TB6523C / 26C / 27C / 28C)

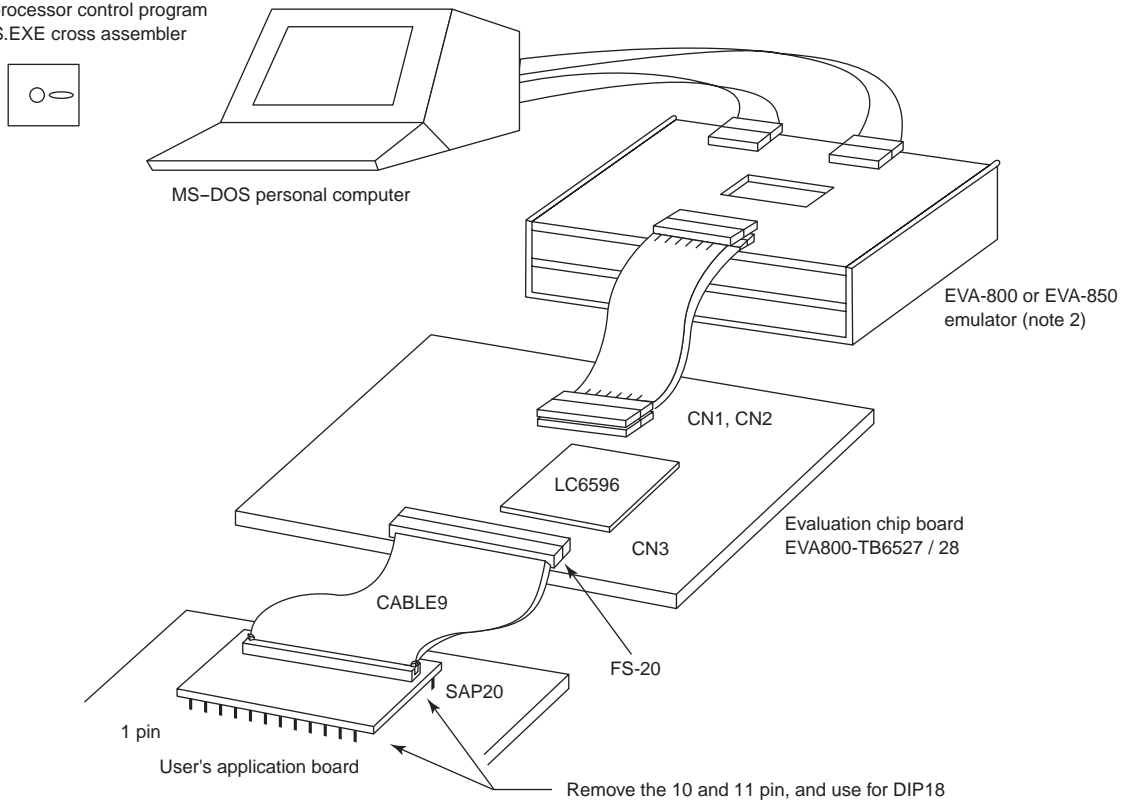
Fig. 2 Program evaluation

D. For program development (EVA-800 or EVA-850 system)

1. MS-DOS for host system (Note 1)
2. Cross assembler.....MS-DOS base cross assembler : <LC65S.EXE>
3. Host control program
4. Evaluation chip : LC6596
5. Emulator : EVA-800 or EVA-850 emulator and evaluation boards EVA800-TB6527 / 28

Appearance of Development Support System

- Host processor control program
- LC65S.EXE cross assembler



ILC00143

(Note 1) MS-DOS : Trademark of Microsoft Corporation

(Note 2) The EVA-800, EVA-850 are general term for emulator. A suffix (A, B,...) is added at the end of EVA-800 and EVA-850 as they are improved to be a newer version. Do not use the EVA-800 and EVA-850 with no suffix added.

LC6527N/F/L, 6528N/F/L

Pin Description

Pin name	Pins	I / O	Function	Option	Reset Mode
VDD	1	–	Power supply	–	–
VSS	1	–			
OSC1	1	Input	<ul style="list-style-type: none"> • Pin for externally connecting RC, ceramic resonator for system clock generation. • For 1-pin external clock input, the PH0 / OSC2 pin is used as I / O port PH0. • For 2-pin RC OSC, 2-pin ceramic resonator OSC, the PH0 / OSC2 pin is used as OSC pin OSC2. 	<ol style="list-style-type: none"> 1-pin external clock input 2-pin RC OSC 2-pin ceramic resonator OSC Predivider option <ol style="list-style-type: none"> No predivider 1 / 3 predivider 1 / 4 predivider 	–
PA 0 to PA3	4	Input / output	<ul style="list-style-type: none"> • I / O port A0 to 3 4-bit input (IP instruction) 4-bit output (OP instruction) Single-bit decision (BP, BNP instruction) Single-bit set / reset (SPB, RPB instruction) • Standby is controlled by PA3. • The PA3 pin must be free from chattering during the HALT instruction execution cycle. 	<ol style="list-style-type: none"> Open drain type output With pull-up resistor 1), 2) : Specified bit by bit	<ul style="list-style-type: none"> • “H” output (Output Nch transistor : OFF)
PC0 to PC3	4	Input / output	<ul style="list-style-type: none"> • I / O port C0 to 3 same as for PA0 to 3 (Note) • Option permits output at the reset mode to be “H” or “L”. (Note) No standby control function is provided. 	<ol style="list-style-type: none"> Open drain type output With pull-up resistor Output at reset mode : “H” Output at reset mode : “L” <ul style="list-style-type: none"> • 1), 2) : Specified bit by bit • 3), 4) : Specified in a group of 4 bits 	<ul style="list-style-type: none"> • “H” output • “L” output (Option-selectable)
PD0 to PD3	4	Input / output	<ul style="list-style-type: none"> • I / O port D0 to 3 Same as for PC0 to 3 	Same as for PC0 to 3	Same as for PC0 to 3
PH0 / OSC2	1	Input / output	<ul style="list-style-type: none"> • I / O port H0 Same as for PA0 to 3 (Note) • Single-bit configuration • For 2-pin OSC, this pin is used as the OSC2 pin, providing no function as I / O port. (Note) No standby control function is provided 	Same as for PA0 to 3	Same as for PA0 to 3
RES	1	Input	<ul style="list-style-type: none"> • System reset input • For power-up reset, C is connected externally. • For reset restart, “L” level is applied for 4 clock cycles or more. 		
TEST	1	Input	<ul style="list-style-type: none"> • LSI test pin Normally connected to VSS 		

Oscillator circuit option

Option Name	Circuit	Conditions, etc.
1. External clock	<p>ILC00102</p>	The PH0 / OSC2 pin is used as port PH0.
2. 2-pin RC OSC	<p>ILC00144</p>	The PH0 / OSC2 pin is used as OSC pin OSC2, providing no function as port.
3. Ceramic resonator OSC	<p>ILC00145</p>	The PH0 / OSC2 pin is used as OSC pin OSC2, providing no function as port.

Predivider Option

Option Name	Circuit	Conditions, etc.
1. No predivider (1 / 1)	<p>ILC00105</p>	<ul style="list-style-type: none"> • Applicable to all of 3 OSC options. • The OSC frequency, external clock do not exceed 1444kHz. (LC6527N, 6528N) • The OSC frequency, external clock do not exceed 4330kHz. (LC6527F, 6528F) • The OSC frequency, external clock do not exceed 1040kHz. (LC6527L, 6528L)
2. 1 / 3 predivider	<p>ILC00106</p>	<ul style="list-style-type: none"> • Applicable to only 2 OSC options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330kHz.
3. 1 / 4 predivider	<p>ILC00107</p>	<ul style="list-style-type: none"> • Applicable to only 2 OSC options of external clock, ceramic resonator OSC. • The OSC frequency, external clock do not exceed 4330kHz.

Note : The OSC option and predivider option are summarized below. Full care must be exercised.

LC6527N/F/L, 6528N/F/L

Table of OSC, predivider Option of LC6527N / 28N, 27F / 28F and 27L / 28L

LC6527N, LC6528N

Circuit Configuration	Frequency	Predivider Option (Cycle time)	VDD Range	Remarks
Ceramic resonator OSC	400kHz	1 / 1 (10 μ s)	3 to 6V	Unusable with 1 / 3, 1 / 4 predivider
	800kHz	1 / 1 (5 μ s)	4 to 6V	
		1 / 3 (15 μ s)	4 to 6V	
	1MHz	1 / 4 (20 μ s)	4 to 6V	
1 / 1 (4 μ s)		4 to 6V		
1-pin external clock	200k to 677kHz	1 / 3 (12 μ s)	4 to 6V	Unusable with 1 / 1 predivider
		1 / 4 (16 μ s)	4 to 6V	
	4kHz	1 / 3 (3 μ s)	4 to 6V	
		1 / 4 (4 μ s)	4 to 6V	
1-pin external clock	600k to 2000kHz	1 / 1 (20 to 6 μ s)	3 to 6V	
	800k to 2667kHz	1 / 3 (20 to 6 μ s)	3 to 6V	
	200k to 1444kHz	1 / 4 (20 to 6 μ s)	3 to 6V	
	600k to 4330kHz	1 / 1 (20 to 2.77 μ s)	4 to 6V	
	800k to 4330kHz	1 / 3 (20 to 2.77 μ s)	4 to 6V	
	800k to 4330kHz	1 / 4 (20 to 3.70 μ s)	4 to 6V	
External clock by 2-pin RC OSC circuit	Same as above			
2-pin RC	Used with 1 / 1 predivider, recommended constants. If used with other than recommended constants, the frequency, predivider option, VDD range must be the same as for 1-pin external clock.		3 to 6V 4 to 6V	
External clock input to the ceramic oscillation circuit	The ceramic oscillation circuit cannot be driven by external clock. To drive the circuit with external clock, select the external clock option or the 2-pin RC option.			

LC6527F, LC6528F

Circuit Configuration	Frequency	Predivider Option (Cycle time)	VDD Range	Remarks
Ceramic resonator OSC	4MHz	1 / 1 (1 μ s)	4.5 to 6V	
1-pin external clock	200k to 4330kHz	1 / 1 (20 to 0.92 μ s)	4.5 to 6V	
External clock input to the ceramic oscillation circuit	The ceramic oscillation circuit cannot be driven by external clock. To drive the circuit with external clock, select the external clock option.			

LC6527N/F/L, 6528N/F/L

LC6527L, LC6528L

Circuit Configuration	Frequency	Predivider Option (Cycle time)	VDD Range	Remarks
Ceramic resonator OSC	400kHz	1 / 1 (10 μ s)	2.2 to 6V	Unusable with 1 / 3, 1 / 4 predivider
	800kHz	1 / 1 (5 μ s)	2.2 to 6V	
		1 / 3 (15 μ s)	2.2 to 6V	
	1MHz	1 / 1 (4 μ s)	2.2 to 6V	2.2 to 6V
1 / 3 (12 μ s)		2.2 to 6V		
4kHz	1 / 4 (20 μ s)	2.2 to 6V	2.2 to 6V	Unusable with 1 / 1, 1 / 3 predivider
	1 / 4 (4 μ s)	2.2 to 6V		
1-pin external clock	200k to 1040kHz 600k to 3120kHz 800k to 4160kHz	1 / 1 (20 to 3.84 μ s) 1 / 3 (20 to 3.84 μ s) 1 / 4 (20 to 3.84 μ s)	2.2 to 6V 2.2 to 6V 2.2 to 6V	
External clock by 2-pin RC OSC circuit	Same as above			
2-pin RC	Used with 1 / 1 predivider, recommended constants. If used with other than recommended constants, the frequency, predivider option, VDD range must be the same as for 1-pin external clock.		2.2 to 6V	
External clock input to the ceramic oscillation circuit	The ceramic oscillation circuit cannot be driven by external clock. To drive the circuit with external clock, select the external clock option or the 2-pin RC option.			

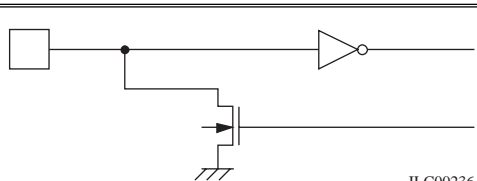
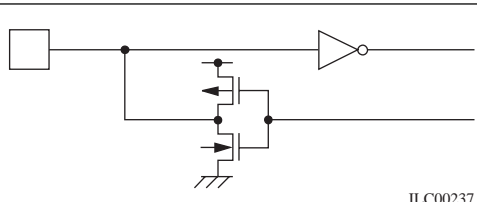
Option of ports C, D Output Level at the Reset Mode

For input / output common ports C, D either of the following two output levels may be selected in a group of 4 bits during reset by option.

Option Name	Conditions, etc.
1. Output at the reset mode : "H" level	All of 4 bits of ports C, D
2. Output at the reset mode : "L" level	All of 4 bits of ports C, D

Option of port Output Configuration

For each input / output common port, either of the following two output configurations may be selected by option.

Option Name	Circuit	Conditions, etc.
1. Open drain output	 <p style="text-align: right; font-size: small;">ILC00236</p>	<ul style="list-style-type: none"> Unapplicable to port PH0 / OSC2 when 2-pin RC OSC or ceramic resonator OSC is selected.
2. Output with pull-up resistor	 <p style="text-align: right; font-size: small;">ILC00237</p>	

LC6527N/F/L, 6528N/F/L

LC6527N, LC6528N

1. Absolute Maximum Ratings at Ta=25°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Limits	unit
Maximum supply voltage	VDD max	VDD		-0.3 to +7.0V	V
Output voltage	VO	OSC2		Allowable up to voltage generated	V
Input voltage	VI(1)	OSC1 (*1)		-0.3 to VDD+0.3	V
	VI(2)	TEST, RES		-0.3 to VDD+0.3	V
Input / output voltage	VIO(1)	Port of OD type		-0.3 to +15	V
	VIO(2)	Port of PU type		-0.3 to VDD+0.3	V
Peak output current	IOP	I / O port		-2 to +20	mA
Average output current	IOA	I / O port	Per pin over the period of 100ms	-2 to +20	mA
	ΣIOA(1)	PA0 to 3	Total current of PA0 to 3, (*2)	-6 to +40	mA
	ΣIOA(2)	PC0 to 3 PH0 PD0 to 3	Total current of PC0 to 3, PD0 to 3 PH0 (*2)	-14 to +90	mA
Allowable power dissipation	Pd max(1)		Ta=-40 to +85°C (DIP package)	300	mW
	Pd max(2)		Ta=-40 to +85°C (MFP package)*	200	mW
Operating temperature	Topg			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	°C

*.....Under development. Do not immerse the package in the solder dip tank when mounting the MFP on the substrate.

2. Allowable Operating Conditions at Ta=-40°C to +85°C, VSS= 0V, VDD=3.0 to 6.0V

Parameter	Symbol	Pins	Conditions	Ratings			unit	
				VDD [V]	min	typ		max
Operating supply voltage	VDD	VDD			3.0		6.0	V
Standby supply voltage	VST	VDD	RAM, register hold (*3)		1.8		6.0	V
“H”-level input voltage	VIH(1)	Port of OD type (except H0)	Output Nch Tr. OFF		0.7VDD		+13.5	V
	VIH(2)	Port of PU type (except H0)	Output Nch Tr. OFF		0.7VDD		VDD	V
	VIH(3)	H0 of OD type	Output Nch Tr. OFF		0.8VDD		+13.5	V
	VIH(4)	H0 of PU type	Output Nch Tr. OFF		0.8VDD		VDD	V
	VIH(5)	RES			0.8VDD		VDD	V
	VIH(6)	OSC1	External clock mode		0.8VDD		VDD	V
“L”-level input voltage	VIL(1)	Port	Output Nch Tr. OFF	VDD=4 to 6	VSS		0.3VDD	V
	VIL(2)	Port	Output Nch Tr. OFF	VDD=3 to 6	VSS		0.25VDD	V
	VIL(3)	OSC1	External clock mode	VDD=4 to 6	VSS		0.25VDD	V
	VIL(4)	OSC1	External clock mode	VDD=3 to 6	VSS		0.2VDD	V
	VIL(5)	TEST		VDD=4 to 6	VSS		0.3VDD	V
	VIL(6)	TEST		VDD=3 to 6	VSS		0.25VDD	V
	VIL(7)	RES		VDD=4 to 6	VSS		0.25VDD	V
	VIL(8)	RES		VDD=3 to 6	VSS		0.2VDD	V

LC6527N/F/L, 6528N/F/L

Parameter	Symbol	Pins	Conditions	VDD [V]	Ratings			unit
					min	typ	max	
Operating frequency (cycle time)	fop (Tcyc)		When the 1 / 3 or 1 / 4 predivider option is selected, clock must not exceed 4.33MHz.	VDD=4 to 6	200		1444	kHz
					(20)		(2.77)	(μ s)
External clock conditions Frequency	text	OSC1	Fig.1. When clock exceeds 1.444MHz, the 1 / 3 or 1 / 4 predivider option is selected.	VDD=4 to 6 3 to 6	200		4330	kHz
					200		2667	kHz
Pulse width	textH, textL	OSC1		VDD=4 to 6 3 to 6	69			ns
Rise / Fall time	textR, textF	OSC1		VDD=4 to 6 3 to 6	180		50	ns
Oscillation guaranty constants 2-pin RC oscillation	Cext	OSC1, OSC2	Fig.2	VDD=3 to 6			220 \pm 5%	pF
	Cext	OSC1, OSC2	Fig.2	VDD=4 to 6			220 \pm 5%	pF
	Rext	OSC1, OSC2	Fig.2	VDD=3 to 6			12 \pm 1%	k Ω
	Rext	OSC1, OSC2	Fig.2	VDD=4 to 6			4.7 \pm 1%	k Ω
Ceramic resonator OSC			Fig.3				Table 1	

3. Electrical Characteristics at Ta=-40°C to +85°C, VSS= 0V, VDD=3.0V to 6.0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
“H”-level input current	I _{IH} (1)	Port of OD type	Output Nch Tr. OFF (including OFF leak current of Nch Tr.) V _{IN} = \pm 13.5V			+5.0	μ A
	I _{IH} (2)	OSC1	External clock mode, V _{IN} =VDD			+1.0	μ A
“L”-level input current	I _{IL} (1)	Port of OD type	Output Nch Tr. OFF V _{IN} =VSS	-1.0			μ A
	I _{IL} (2)	Port of PU type	Output Nch Tr. OFF V _{IN} =VSS	-1.3	-0.35		mA
	I _{IL} (3)	$\overline{\text{RES}}$	V _{IN} =VSS	-45	-10		μ A
	I _{IL} (4)	OSC1	External clock mode, V _{IN} =VSS	-1.0			μ A
“H”-level output voltage	V _{OH} (1)	Port of PU type	I _{OH} =-50 μ A VDD=4.0V to 6.0V	VDD-1.2			V
	V _{OH} (2)	Port of PU type	I _{OH} =-10 μ A	VDD-0.5			V
“L”-level output voltage	V _{OL} (1)	Port	I _{OL} =10mA VDD=4.0V to 6.0V			1.5	V
	V _{OL} (2)	Port	I _{OL} =1.8mA, I _{OL} of each port : 1mA or less			0.4	V
Hysteresis voltage	V _{HIS}	$\overline{\text{RES}}$, OSC1 of schmitt type(*4)			0.1VDD		V

LC6527N/F/L, 6528N/F/L

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Current dissipation 2-pin RC oscillation	IDDOP(1)	VDD	Output Nch Tr. OFF at operating, Port=VDD Fig.2 fosc=850kHz (TYP) VDD=4 to 6V		1.5	4	mA
	IDDOP(2)	VDD	Fig.2 fosc=400kHz (TYP)		1.0	4	mA
Ceramic resonator oscillation	IDDOP(3)	VDD	Fig.3 4MHz, 1 / 3 predivider VDD=4 to 6V		2.0	5	mA
	IDDOP(4)	VDD	Fig.3 4MHz, 1 / 4 predivider VDD=4 to 6V		2.0	4	mA
External clock	IDDOP(5)	VDD	Fig.3 400kHz		0.5	2	mA
	IDDOP(6)	VDD	Fig.3 800kHz VDD=4 to 6V		1.5	4	mA
	IDDOP(7)	VDD	200kHz to 667kHz, 1 / 1 predivider 600kHz to 2000kHz, 1 / 3 predivider 800kHz to 2667kHz, 1 / 4 predivider		1.5	4	mA
	IDDOP(8)	VDD	200kHz to 1444kHz, 1 / 1 predivider 600kHz to 4330kHz, 1 / 3 predivider 800kHz to 4330kHz, 1 / 4 predivider VDD=4 to 6V		2.0	5	mA
Standby mode	IDDst	VDD	Output Nch Tr. OFF VDD=6V		0.05	10	μA
		VDD	Port=VDD VDD=3V		0.025	5	μA
Oscillation characteristics Ceramic OSC Frequency	fCFOSC (*5)	OSC1, OSC2	Fig.3 fo=400kHz	384	400	416	kHz
		OSC1, OSC2	Fig.3 fo=800kHz, VDD=4 to 6V	768	800	832	kHz
		OSC1, OSC2	Fig.3 fo=1MHz, VDD=4 to 6V	960	1000	1040	kHz
		OSC1, OSC2	Fig.3 fo=4MHz, 1 / 3 predivider 1 / 4 predivider, VDD=4 to 6V	3840	4000	4160	kHz
Stable time	tCFS		Fig.4 fo=400kHz			10	ms
			Fig.4 fo=800kHz, 1MHz, 4MHz, 1 / 3 predivider, 1 / 4 predivider VDD=4 to 6V			10	ms
2-pin RC oscillation Frequency	fMOSC	OSC1, OSC2	Fig.2 Cext=220pF±5% Fig.2 Rext=4.7kΩ±1% VDD=4 to 6V	646	850	1117	kHz
		OSC1, OSC2	Fig.2 Cext=220pF±5% Fig.2 Rext=12kΩ±1% VDD=3 to 6V	304	400	580	kHz

LC6527N/F/L, 6528N/F/L

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Pull-up resistance I / O port pull-up resistance	RPP	Port of PU type	VDD=5V		14		kΩ
External reset characteristics Reset time	tRST				See Fig.5		
Pin capacitance	Cp		f=1MHz Other than pins to be tested, VIN=VSS		10		pF

- (*1) When oscillated internally under the oscillating conditions in Fig.3, up to the oscillation amplitude generated is allowable.
- (*2) Average over the period of 100ms.
- (*3) Operating supply voltage VDD must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.
- (*4) The OSC1 pin can be schmitt-triggered when the 2-pin RC oscillation option or external clock oscillation option has been selected.
- (*5) fCFOSC : oscillation frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic resonator mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

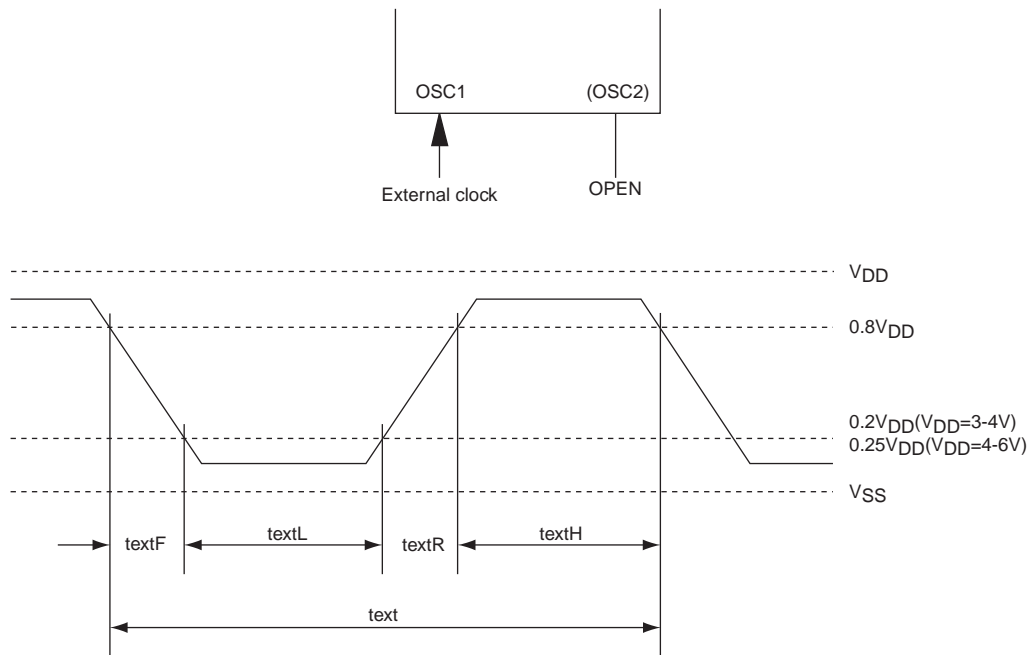


Fig. 1 External Clock Input Waveform

ILC00146

*External clock can be used at selecting 2-pin RC option or 1-pin external clock option, and cannot be used at ceramic resonator oscillation.

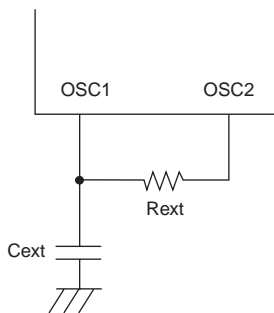


Fig. 2 2-pin RC Oscillation Circuit

ILC00088

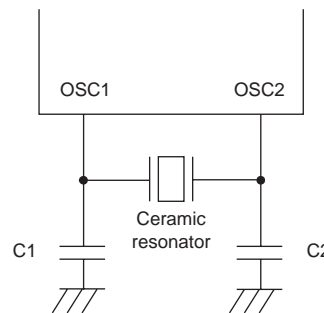


Fig. 3 Ceramic Resonator Oscillation Circuit

ILC00147

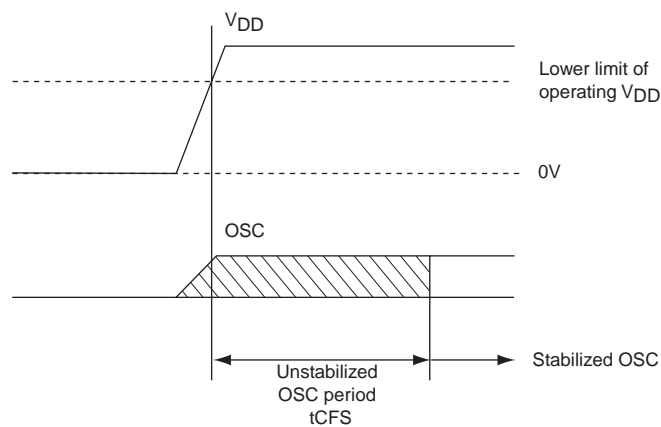


Fig. 4 Oscillation Stabilizing Period

ILC00148

Table 1 Constants Guaranteed for
Ceramic Resonator OSC

4MHz (Murata) CSA4.00MG	C1	33pF±10%
	C2	33pF±10%
	R	0Ω
4MHz (Kyocera) KBR4.0MSA	C1	33pF±10%
	C2	33pF±10%
	R	0Ω
4MHz (Kyocera) KBR4.0MKS (built-in C)	C1	100pF±10%
	C2	100pF±10%
	R	2.2Ω
1MHz (Murata) CSB1000J	C1	100pF±10%
	C2	100pF±10%
	R	0Ω
1MHz (Kyocera) KBR1000F	C1	100pF±10%
	C2	100pF±10%
	R	0Ω
800kHz (Murata) CSB800J	C1	100pF±10%
	C2	100pF±10%
	R	2.2Ω
800kHz (Kyocera) KBR800F	C1	100pF±10%
	C2	100pF±10%
	R	0Ω
400kHz (Murata) CSB400P	C1	220pF±10%
	C2	220pF±10%
	R	2.2Ω
400kHz (Kyocera) KBR400BK	C1	330pF±10%
	C2	330pF±10%
	R	0Ω

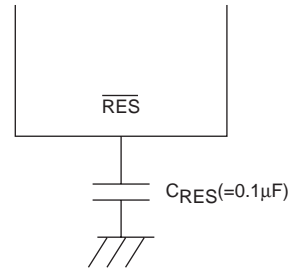


Fig. 5 Reset Circuit

ILC00240

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at $C_{RES}=0.1\mu F$. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or more.

LC6527N/F/L, 6528N/F/L

RC Oscillation Characteristics of the LC6527N, LC6528N

Fig. 6 shows the RC oscillation characteristics of the LC6527N, LC6528N. For the variation range of RC OSC frequency of the LC6527N, LC6528N, the following are guaranteed at the external constants only shown below.

- 1) $V_{DD}=3.0V$ to $6.0V$, $T_a=-40^{\circ}C$ to $+85^{\circ}C$
 External constants $C_{ext}=220pF$
 $R_{ext}=12k\Omega$
 $304kHz \leq f_{MOSC} \leq 580kHz$
- 2) $V_{DD}=4.0V$ to $6.0V$, $T_a=-40^{\circ}C$ to $+85^{\circ}C$
 $C_{ext}=220pF$
 $R_{ext}=4.7k\Omega$
 $646kHz \leq f_{MOSC} \leq 1117kHz$

If any other constants than specified above are used, the range of $R_{ext}=3k\Omega$ to $20k\Omega$, $C_{ext}=150pF$ to $390pF$ must be observed. (See Fig.6.)

- (*6) : The oscillation frequency at $V_{DD}=5.0V$, $T_a=+25^{\circ}C$ must be in the range of $350kHz$ to $750kHz$.
- (*7) : The oscillation frequency at $V_{DD}=4.0V$ to $6.0V$, $T_a=-40^{\circ}C$ to $+85^{\circ}C$ and $V_{DD}=3.0V$ to $6.0V$, $T_a=-40^{\circ}C$ to $85^{\circ}C$ must be within the operation clock frequency range.

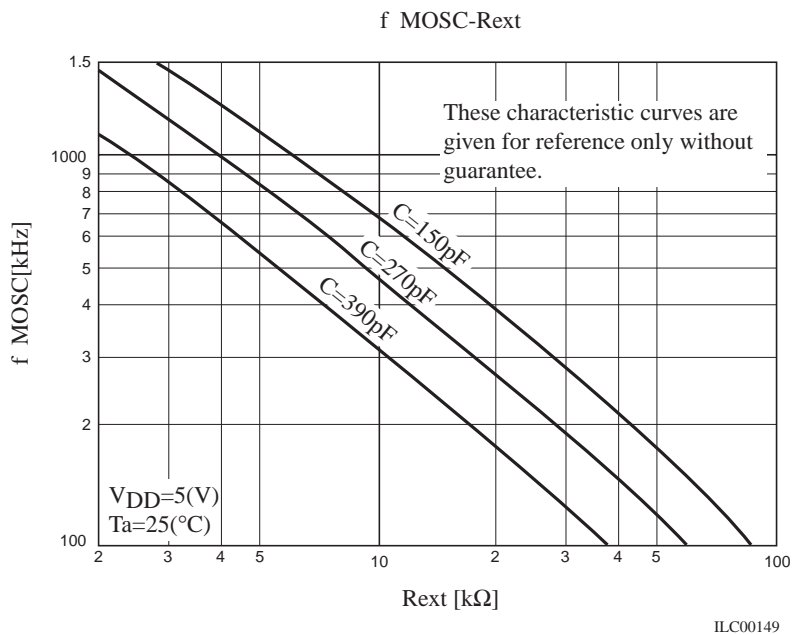


Fig. 6 RC Oscillation Frequency Data (Typ.)

LC6527N/F/L, 6528N/F/L

LC6527F, LC6528F

1. Absolute Maximum Ratings at Ta=25°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Limits	unit
Maximum supply voltage	VDD max	VDD		-0.3 to +7.0V	V
Output voltage	VO	OSC2		Allowable up to voltage generated	V
Input voltage	VI(1)	OSC1 (*1)		-0.3 to VDD+0.3	V
	VI(2)	TEST, RES		-0.3 to VDD+0.3	V
Output voltage	VIO(1)	Port of OD type		-0.3 to +15	V
	VIO(2)	Port of PU type		-0.3 to VDD+0.3	V
Peak output current	IOP	I / O port		-2 to +20	mA
Average output current	IOA	I / O port	Per pin over the period of 100ms	-2 to +20	mA
	ΣIOA(1)	PA0 to 3	Total current of PA0 to 3, (*2)	-6 to +40	mA
	ΣIOA(2)	PC0 to 3 PH0 PD0 to 3	Total current of PC0 to 3, PD0 to 3, PH0 (*2)	-14 to +90	mA
Allowable power dissipation	Pd max(1)		Ta=-40 to +85°C (DIP package)	300	mW
	Pd max(2)		Ta=-40 to +85°C (MFP package)*	200	mW
Operating temperature	Topg			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	°C

*.....Under development. Do not immerse the package in the solder dip tank when mounting the MFP on the substrate.

2. Allowable Operating Conditions at Ta=-40°C to +85°C, VSS= 0V, VDD=4.5 to 6.0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Operating supply voltage	VDD	VDD		4.5		6.0	V
Standby supply voltage	VST	VDD	RAM, register hold (*3)	1.8		6.0	V
“H”-level input voltage	VIH(1)	Port of OD type (except H0)	Output Nch Tr. OFF	0.7VDD		+13.5	V
	VIH(2)	Port of PU type (except H0)	Output Nch Tr. OFF	0.7VDD		VDD	V
	VIH(3)	H0 of OD type	Output Nch Tr. OFF	0.8VDD		+13.5	V
	VIH(4)	H0 of PU type	Output Nch Tr. OFF	0.8VDD		VDD	V
	VIH(5)	RES		0.8VDD		VDD	V
	VIH(6)	OSC1	External clock mode	0.8VDD		VDD	V
“L”-level input voltage	VIL(1)	Port	Output Nch Tr. OFF	VSS		0.3VDD	V
	VIL(2)	OSC1	External clock mode	VSS		0.25VDD	V
	VIL(3)	TEST		VSS		0.3VDD	V
	VIL(4)	RES		VSS		0.25VDD	V

LC6527N/F/L, 6528N/F/L

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Operating frequency (Cycle time)	fop (Tcyc)			200 (20)		4330 (0.92)	kHz (μs)
External clock conditions							
Frequency	text	OSC1	} Fig.1	200		4330	kHz
Pulse width	textH, textL	OSC1		69			ns
Rise / Fall time	textR, textF	OSC1				50	ns
Oscillation guaranteed constants ceramic resonator OSC			Fig.2	See Table 1			

3. Electrical Characteristics at Ta=-40°C to +85°C, VSS= 0V, VDD=4.5V to 6.0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
“H”-level input current	I _{IH} (1)	Port of OD type	Output Nch Tr. OFF (including OFF leak current of Nch Tr.) V _{IN} =±13.5V			+5.0	μA
	I _{IH} (2)	OSC1	External clock mode, V _{IN} =VDD			+1.0	μA
“L”-level input current	I _{IL} (1)	Port of OD type	Output Nch Tr. OFF V _{IN} =VSS	-1.0			μA
	I _{IL} (2)	Port of PU type	Output Nch Tr. OFF V _{IN} =VSS	-1.3	-0.35		mA
	I _{IL} (3)	RES	V _{IN} =VSS	-45	-10		μA
	I _{IL} (4)	OSC1	External clock mode, V _{IN} =VSS	-1.0			μA
“H”-level output voltage	V _{OH} (1)	Port of PU type	I _{OH} =-50μA	VDD-1.2			V
	V _{OH} (2)	Port of PU type	I _{OH} =-10μA	VDD-0.5			V
“L”-level output voltage	V _{OL} (1)	Port	I _{OL} =10mA			1.5	V
	V _{OL} (2)	Port	I _{OL} =1.8mA, I _{OL} of each port : 1mA or less			0.4	V
Hysteresis voltage	V _{HIS}	RES, OSC1 of schmitt type(*4)			0.1VDD		V

LC6527N/F/L, 6528N/F/L

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Current dissipation Ceramic resonator OSC	IDDOP(1)	VDD	Fig.2 4MHz		1.5	3.5	mA
External clock	IDDOP(2)	VDD	200kHz to 4330kHz *1 Output Nch Tr.OFF at Operating mode Port=VDD		1.5	3.5	mA
Standby mode	IDDst	VDD	Output Nch Tr. OFF VDD=6V		0.05	10	μA
		VDD	Port=VDD VDD=3V		0.025	5	μA
Oscillation characteristics Ceramic OSC							
Frequency	fCFOSC	OSC1, OSC2	Fig.2 fo=4MHz (*5)	3840	4000	4160	kHz
Stable time	tCFS		Fig.3 fo=4MHz			10	ms
Pull-up resistance I / O port pull-up resistance	RPP	Port of PU type	VDD=5V		14		kΩ
External reset characteristics Reset time	tRST				See Fig.4		
Pin capacitance	Cp		f=1MHz, other than pins to be tested, VIN=VSS		10		pF

- (*1) When oscillated internally under the oscillating conditions in Fig.2, up to the oscillation amplitude generated is allowable.
- (*2) Average over the period of 100ms.
- (*3) Operating supply voltage VDD must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.
- (*4) The OSC1 pin can be schmitt-triggered when the external clock oscillation option has been selected.
- (*5) fCFOSC : Oscillatable frequency.

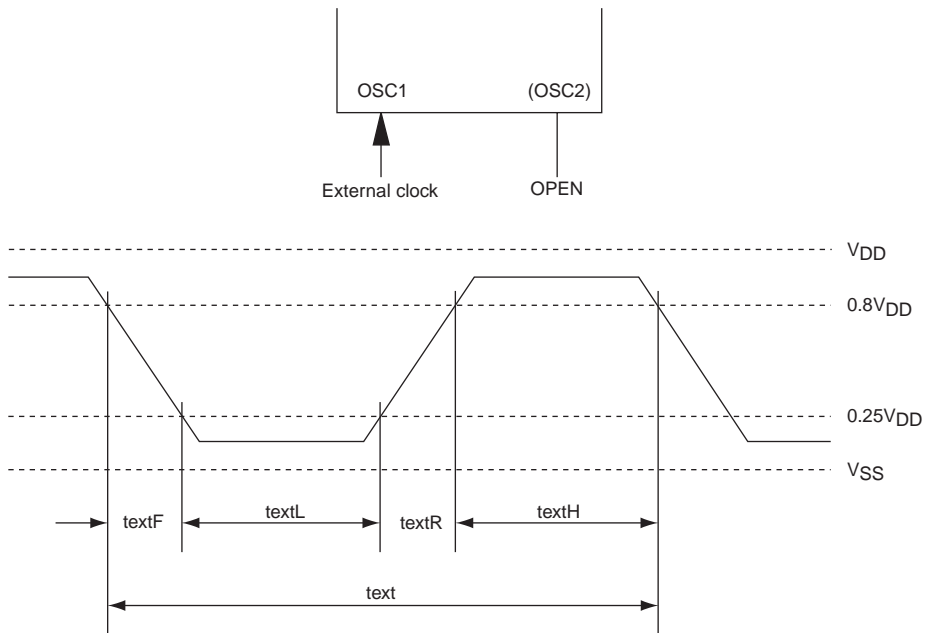


Fig. 1 External Clock Input Waveform

ILC00150

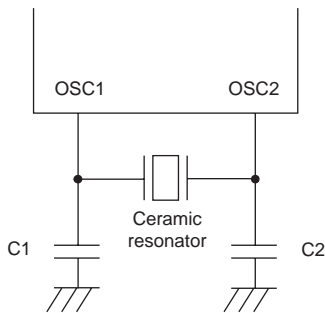


Fig. 2 Ceramic Resonator OSC Circuit ILC00151

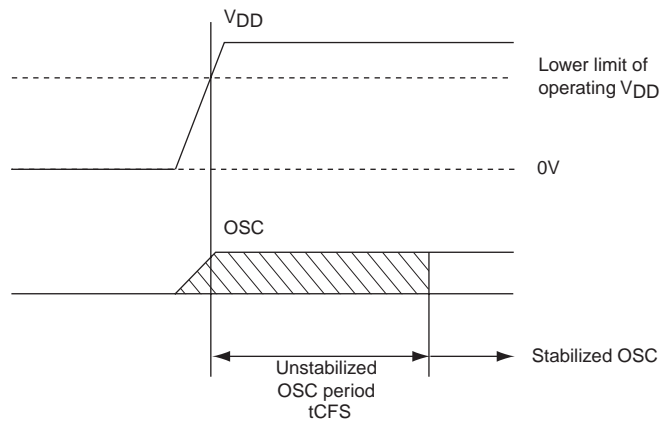


Fig. 3 OSC Stabilizing Period

ILC00152

Table 1 Constants Guaranteed for Ceramic Resonator OSC

4MHz (Murarta) CSA4.00MG	C1	33pF±10%
	C2	33pF±10%
	R	0Ω
4MHz (Kyocera) KBR4.0MSA KBR4.0MKS (built-in C)	C1	33pF±10%
	C2	33pF±10%
	R	0Ω

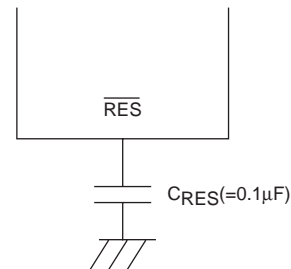


Fig. 4 Reset Circuit

ILC00153

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at $C_{RES}=0.1\mu F$. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or more.

LC6527N/F/L, 6528N/F/L

LC6527L, LC6528L

1. Absolute Maximum Ratings at Ta=25°C, VSS=0V

Parameter	Symbol	Pins	Conditions	Limits	unit
Maximum supply voltage	VDD max	VDD		-0.3 to +7.0	V
Output voltage	VO	OSC2		Allowable up to voltage generated	V
Input voltage	VI(1)	OSC1 (*1)		-0.3 to VDD+0.3	V
	VI(2)	TEST, RES		-0.3 to VDD+0.3	V
Input / output voltage	VIO(1)	Port of OD type		-0.3 to +15	V
	VIO(2)	Port of PU type		-0.3 to VDD+0.3	V
Peak output current	IOP	I / O port		-2 to +20	mA
Average output current	IOA	I / O port	Per pin over the period of 100ms	-2 to +20	mA
	ΣIOA(1)	PA0 to 3	Total current of PA0 to 3, (*2)	-6 to +40	mA
	ΣIOA(2)	PC0 to 3 PH0 PD0 to 3	Total current of PC0 to 3, PD0 to 3 PH0 (*2)	-14 to +90	mA
Allowable power dissipation	Pd max(1)		Ta=-40 to +85°C (DIP package)	250	mW
	Pd max(2)		Ta=-40 to +85°C (MFP package)*	150	mW
Operating temperature	Topg			-40 to +85	°C
Storage temperature	Tstg			-55 to +125	°C

*.....Under development. Do not immerse the package in the solder dip tank when mounting the MFP on the substrate.

2. Allowable Operating Conditions at Ta=-40°C to 85°C, VSS= 0V, VDD=2.2 to 6.0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Operating supply voltage	VDD	VDD		2.2		6.0	V
Standby supply voltage	VST	VDD	RAM, register hold (*3)	1.8		6.0	V
“H”-level input voltage	VIH(1)	Port of OD type (except H0)	Output Nch Tr. OFF	0.7VDD		+13.5	V
	VIH(2)	Port of PU type (except H0)	Output Nch Tr. OFF	0.7VDD		VDD	V
	VIH(3)	H0 of OD type	Output Nch Tr. OFF	0.8VDD		+13.5	V
	VIH(4)	H0 of PU type	Output Nch Tr. OFF	0.8VDD		VDD	V
	VIH(5)	RES		0.8VDD		VDD	V
	VIH(6)	OSC1	External clock	0.8VDD		VDD	V
“L”-level input voltage	VIL(1)	Port	Output Nch Tr. OFF	VSS		0.2VDD	V
	VIL(2)	OSC1	External clock	VSS		0.15VDD	V
	VIL(3)	TEST		VSS		0.2VDD	V
	VIL(4)	RES		VSS		0.15VDD	V

LC6527N/F/L, 6528N/F/L

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Operating frequency (cycle time)	fop (Tcyc)		When the 1 / 3 or 1 / 4 predivider option is selected, clock must not exceed 4.16MHz.	200 (20)		1040 (3.84)	kHz (μs)
External clock conditions							
Frequency	text	OSC1	Fig.1 When clock exceeds 1.040MHz, the 1 / 3 or 1 / 4 predivider option is selected.	200		4160	kHz
Pulse width	textH, textL	OSC1		100			ns
Rise / fall time	textR, textF	OSC1				100	ns
Oscillation guaranteed constants							
2-pin RC oscillation	Cext	OSC1, OSC2	Fig.2	220±5%			pF
	Rext			12±1%			kΩ
Ceramic oscillation			Fig.3	See Table 1.			

3. Electrical Characteristics at Ta=-40°C to +85°C, VSS=0V, VDD=2.2V to 6.0V

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
“H”-level input current	I _{IH} (1)	Port of OD type	Output Nch Tr. OFF (including OFF leak current of Nch Tr.) V _{IN} =±13.5V			+5.0	μA
	I _{IH} (2)	OSC1	External clock mode, V _{IN} =V _{DD}			+1.0	μA
“L”-level input current	I _{IL} (1)	Port of OD type	Output Nch Tr. OFF V _{IN} =V _{SS}	-1.0			μA
	I _{IL} (2)	Port of PU type	Output Nch Tr. OFF V _{IN} =V _{SS}	-1.3	-0.35		mA
	I _{IL} (3)	RES	V _{IN} =V _{SS}	-45	-10		μA
	I _{IL} (4)	OSC1	External clock mode, V _{IN} =V _{SS}	-1.0			μA
“H”-level output voltage	V _{OH}	Port of PU type	I _{OH} =-10μA	V _{DD} -0.5			V
“L”-level output voltage	V _{OL} (1)	Port	I _{OL} =3mA			1.5	V
	V _{OL} (2)	Port	I _{OL} =1mA, I _{OL} of each port : 1mA or less			0.4	V
Hysteresis voltage	V _{HIS}	RES, OSC1 of schmitt type(*4)		0.1V _{DD}			V

LC6527N/F/L, 6528N/F/L

Parameter	Symbol	Pins	Conditions	Ratings			unit
				min	typ	max	
Current dissipation			Output Nch Tr. OFF at operating, Port=VDD				
2-pin RC OSC	IDDOP(1)	VDD	Fig.2 fOSC=400kHz (TYP)		0.8	2.5	mA
Ceramic OSC	IDDOP(2)	VDD	Fig.3 4MHz, 1 / 4 predivider		1.2	2.5	mA
	IDDOP(3)	VDD	Fig.3 4MHz, 1 / 4 predivider VDD=2.2V		0.5	1	mA
	IDDOP(4)	VDD	Fig.3 400kHz		0.5	2	mA
	IDDOP(5)	VDD	Fig.3 800kHz		1.0	2.5	mA
External clock	IDDOP(6)	VDD	200kHz to 667kHz, 1 / 1 predivider 600kHz to 2000kHz, 1 / 3 predivider 800kHz to 2667kHz, 1 / 4 predivider		1.0	2.5	mA
Standby mode	IDDst	VDD VDD	Output Nch Tr. OFF VDD=6V Port=VDD VDD=2.2V		0.05 0.025	10 5	μA μA
Oscillation characteristics							
Ceramic OSC							
Frequency	fCFOSC (*5)	OSC1, OSC2 OSC1, OSC2 OSC1, OSC2 OSC1, OSC2	Fig.3 fo=400kHz Fig.3 fo=800kHz Fig.3 fo=1MHz Fig.3 fo=4MHz 1 / 4 predivider	384 768 960 3840	400 800 1000 4000	416 832 1040 4160	kHz kHz kHz kHz
Stable time	tCFS		Fig.4 fo=400kHz Fig.4 fo=800kHz, 1MHz, 4MHz, 1 / 4 predivider			10 10	ms ms
2-pin RC OSC	fMOSC	OSC1, OSC2	Fig.2 Cext=220pF±5% Fig.2 Rext=12kΩ±1%	281	400	580	kHz
Frequency							
Pull-up resistance							
I / O port pull-up resistance	RPP	Port of PU type	VDD=5V		14		kΩ
External reset characteristics							
Reset time	tRST			See Fig.5.			
Pin capacitance	Cp		f=1MHz Other than pins to be tested, VIN=VSS		10		pF

- (*1) When oscillated internally under the oscillating conditions in Fig.3, up to the oscillation amplitude generated is allowable.
- (*2) Average over the period of 100ms.
- (*3) Operating supply voltage VDD must be held until the standby mode is entered after the execution of the HALT instruction. The PA3 pin must be free from chattering during the HALT instruction execution cycle.
- (*4) The OSC1 pin can be schmitt-triggered when the 2-pin RC oscillation option or external clock oscillation option has been selected.
- (*5) fCFOSC : Oscillatable frequency. There is a tolerance of approximately 1% between the center frequency at the ceramic resonator mode and the nominal value presented by the ceramic resonator supplier. For details, refer to the specification for the ceramic resonator.

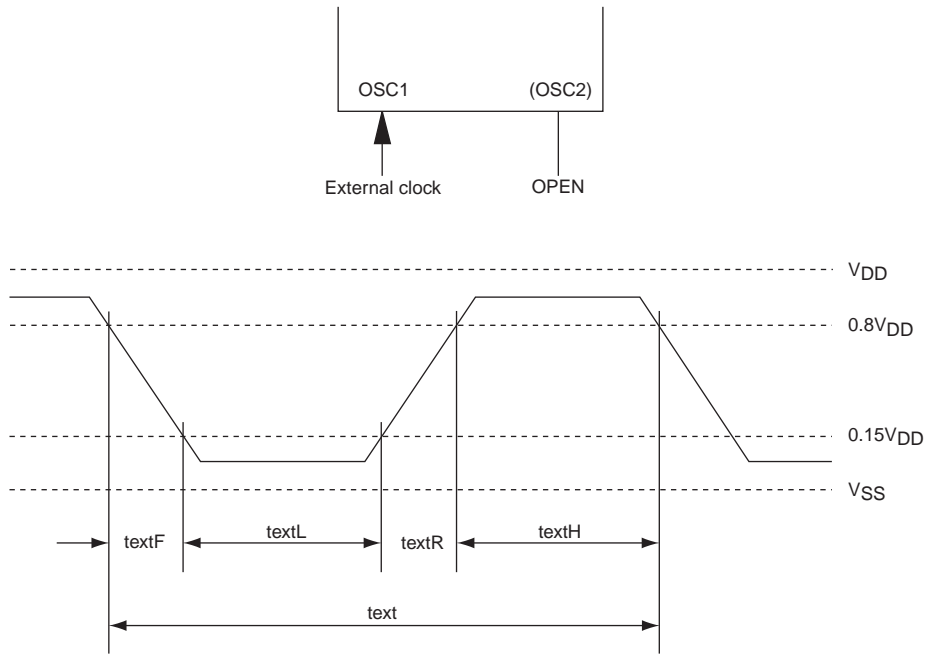


Fig. 1 External Clock Input Waveform

ILC00154

*External clock can be used at selecting 2-pin RC option or 1-pin external clock option, and cannot be used at ceramic resonator oscillation.

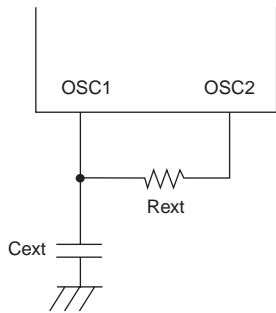


Fig. 2 2-pin RC Oscillation Circuit

ILC00088

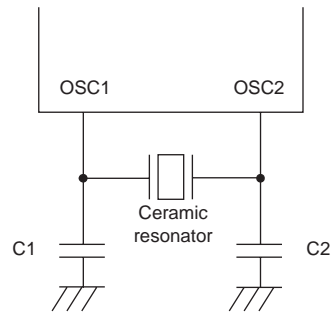


Fig. 3 Ceramic Resonator Oscillation Circuit

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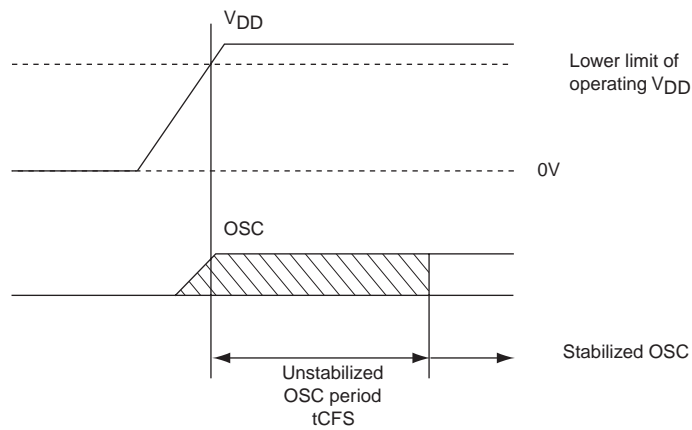


Fig. 4 Oscillation Stabilizing Period

ILC00148

Table 1 Constants Guaranteed for
Ceramic Resonator OSC

4MHz (Murata) CSA4.00MGU	C1	33pF±10%
	C2	33pF±10%
	R	0Ω
CST4.00MGWU (built-in C)	C1	100pF±10%
	C2	100pF±10%
	R	2.2Ω
1MHz (Murata) CSB1000J	C1	100pF±10%
	C2	100pF±10%
	R	0Ω
1MHz (Kyocera) KBR1000F	C1	100pF±10%
	C2	100pF±10%
	R	0Ω
800kHz (Murata) CSB800J	C1	100pF±10%
	C2	100pF±10%
	R	2.2Ω
800kHz (Kyocera) KBR800F	C1	100pF±10%
	C2	100pF±10%
	R	0Ω
400kHz (Murata) CSB400P	C1	220pF±10%
	C2	220pF±10%
	R	2.2Ω
400kHz (Kyocera) KBR400BK	C1	330pF±10%
	C2	330pF±10%
	R	0Ω

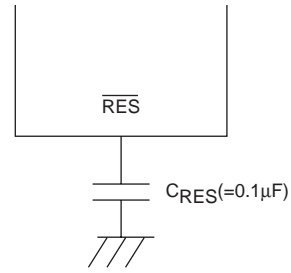


Fig. 5 Reset Circuit

ILC00240

(Note) When the rise time of the power supply is 0, the reset time becomes 10ms to 100ms at $C_{RES}=0.1\mu F$. If the rise time of the power supply is long, the value of C_{RES} must be increased so that the reset time becomes 10ms or more.

LC6527N/F/L, 6528N/F/L

RC Oscillation Characteristic of the LC6527L, LC6528L

Fig. 6 shows the RC oscillation characteristic of the LC6527L, 6528L. For the variation range of RC OSC frequency of the LC6527L, 6528L, the following are guaranteed at the external constants only shown below.

$V_{DD}=2.2V$ to $6.0V$, $T_a=-40^{\circ}C$ to $+85^{\circ}C$

External constants $C_{ext}=220pF$

$R_{ext}=12k\Omega$

$281kHz \leq f_{MOSC} \leq 580kHz$

If any other constants than specified above are used, the range of $R_{ext}=3k\Omega$ to $20k\Omega$, $C_{ext}=150pF$ to $390pF$ must be observed. (See Fig.6.)

(*6) : The oscillation frequency at $V_{DD}=5.0V$, $T_a=+25^{\circ}C$ must be in the range of $350kHz$ to $500kHz$.

(*7) : The oscillation frequency at $V_{DD}=2.2V$ to $6.0V$, $T_a=-40^{\circ}C$ to $+85^{\circ}C$ must be within the operation clock frequency range.

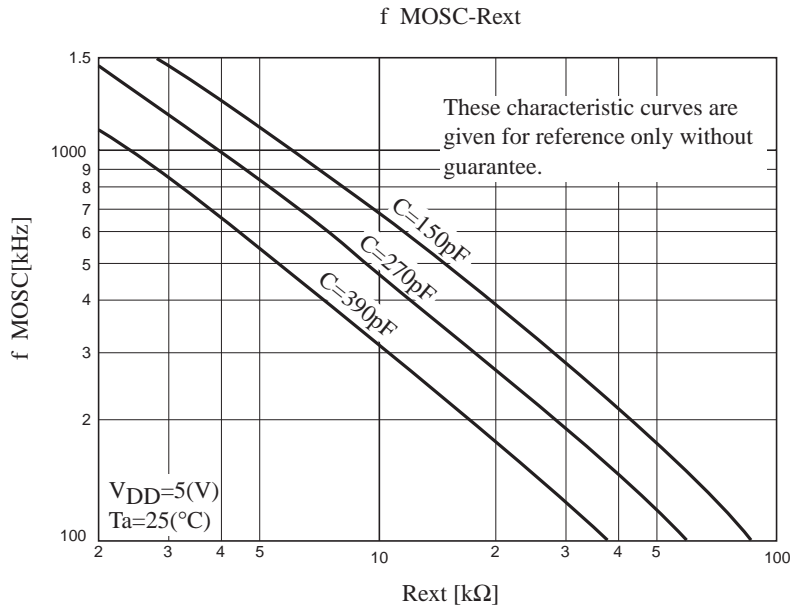


Fig. 6 RC Oscillation Frequency Data (Typ.)

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